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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/681,327	03/19/2001	Jack Robert Smith	BUR920000098US1	9570

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EXAMINER	
VO, TED T	

ART UNIT	PAPER NUMBER
2122	7

DATE MAILED: 12/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/681,327	SMITH ET AL.	
	Examiner	Art Unit	
	Ted T. Vo	2122	

-- Th MAILING DATE of this communication appears on the cover sheet with th correspondence address --

Peri d for R ply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 September 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This action is in response to the amendment filed on 09/05/2003.

Claims 1-5 are amended. Claims 6-20 are canceled.

Regarding the amendment of claims 2-5, the previously claimed objection in accordance to MPEP 714, is withdrawn.

Claim 1-5 are pending in the application.

Response to Arguments

2. Applicants' arguments to the amended claims 1-5 have been considered. However, the arguments are not persuasive.

In the section remarks (page 3), with the amended limitation, "*means for switch an execution of said legacy code by said CPU to an execution of said plurality of optimized code, in response to an encounter of a switch point*"; applicants contend that Chow does not teach this limitation.

Examiner respectfully disagrees: Figure 1, Chows discloses Object Code (legacy code) and Modified Code (a plurality of optimized code), The Instruction Path Coprocessor (I-COP) modifies the Object Code into the Modified Code (page 149, figure 1). Figure 1 shows it has '**interrupt**'. Chow addresses modification techniques in which different code can be selectively and adaptively invoked at runtime (see page 147, right column, second paragraph, lines 10-13; and see page 150, right column, section 2.3, second paragraph). These teach switching mechanism for transferring execution from the core processor to I-COP. "invoked at run-time" (page 147, right column, second paragraph, line13) teaches a switch mechanism in response to an encounter of a switch point.

Claim Rej ctions - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1, 3-5 are rejected under 35 U.S.C. 102(a) as being anticipated by Chow et al., "PipeRench Implementation of the Instruction Path Coprocessor", IEEE, Dec. 2000.

Given the broadest reasonable interpretation of followed claims in light of the specification.

As per claim 1:

Regarding claim limitation: *"A data processing system, comprising:*

A system memory for storing legacy code (page 149, Figure 1, the area containing 'Object Code', page 151, Figure 5, 'I-COP')*;*

a central processing unit (CPU) (figure 1, page 149, core processor) *in communication with said system memory;*

a code-optimizing coprocessor (figure 1, page 149, Instruction Path coprocessor I-COP) *in communication with said system memory and said CPU, wherein said code-optimizing coprocessor generates a plurality of* (figure 1, page 149, backed-arrow, modified instructions) *optimized code* (figure 1, page 149, modified code) *from said legacy code to be stored within said system memory while said CPU is executing said legacy code, wherein said plurality of optimized code is more optimized for execution within said CPU* (see abstract and see page 148, section 2.1.1, 'runs concurrently with core processor', and see page 158, first column, second paragraph, 'based on application behavior) *than said legacy code; and*

means for switching an execution of said legacy code by said CPU to an execution of said plurality of optimized code, (page 149, figure 1, 'interrupt'; page 147, right column, second paragraph, lines 10-13; and page 150, right column, section 2.3, second paragraph).
in response to an encounter of a switch point" (see page 147, second column, second paragraph, "it allows many code modification techniques to be implemented using the same engine, each of which can be selectively and adaptively **invoked at runtime**').

-Chow discloses an architecture (figure 1) which comprises a core processor (CPU) in communication with a memory (figure 1, page 149, Object code). The coprocessor generates optimized code (figure 1, page 149, Instruction Path coprocessor) from object code. The optimized code is stored within trace buffers and within I-COP data memory (Figure 5). It allows the core processor to use the optimized code with a new format that can be more efficiently executed (see abstract).

As per claim 3: Chow teaches the coprocessor that comprises trace buffers ('*a translation look-aside buffer*') that stores optimized code (see page 151, figure 5) and the mechanism of fill buffer, Task Queue, (*PTE*) for optimizing code in the trace buffers (see page 151, Figure 5, and section 3).

As per claim 4: Chow teaches, "*The data processing of claim 3, where said CPU further comprises a program counter, wherein said code-optimizing coprocessor alters said program counter to point to said PTE for said plurality of optimized code after said PTE has been generated for said plurality of optimized code in said TLB, thereby causing said CPU to automatically utilized said plurality of optimized code in lieu of said legacy code*" (see page 151, Figure 5, Core processor points to Fill buffer and Task Queue (PTE) which is for generating optimized code in the trace buffers).

As per claim 5:
Chow discusses the L1 cache and L2 Cache as parts of processor hardware for storing fetched instructions (see page 154, first column, section 4.1).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chow et al., "PipeRench Implementation of the Instruction Path Coprocessor", IEEE, Dec. 2000 in view of Endo et al., (US 6,615,303).

Given the broadest reasonable interpretation of followed claims in light of the specification:

As per claim 2: Chow teaches legacy code which is brought to a coprocessor for optimized and stored in I-COP data memory and trace buffer (see page 151, figure 5, switching mechanism from Core processor to I-COP; and also see page 147, right column, second paragraph, lines 10-13; and see page 150, right column, section 2.3, second paragraph). The teaching covers the switching mechanism that is recited in claim 2, "*The data processing of Claim 1, where said data processing system further includes a switch point table for storing said switch point and other switch points, wherein said switch points identify specific instructions within said legacy code at which execution can be switched from said legacy code to said plurality of optimized code with out any change to an architectural state of said CPU*",
Although Chow disclose switching mechanism as 'interrupt' and 'selectively and adaptively invoked at run time' between object code (Legacy code) and modified code (optimized code) as noted above and as shown by Figure 1 for switching from object code,

Chow does not address "*a switch point table for storing said switch point and other switch points*". Endo disclose an OS context switching (Endo: FIG.5) and an interrupt address table (Endo: FIG.6) for handle a plurality of operating systems (Endo: column 3, lines 5-7).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to include switch table in a switching execution as shown in the teaching of Endo into switching mechanism for handling multi tasks. The motivation is provided for conforming to a standard processor multitasking, particularly in interrupts handling with a tabular manner, for easing addresses management.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Bunnell et al., US 6,075,939 discloses a switch jump table for handling co-execution in multiple process.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ted T. Vo whose telephone number is (703) 308-9049. The examiner can normally be reached on Monday-Friday from 8:00 AM to 5:30 PM ET. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Dam, can be reached on (703) 305-4552.

The fax phone numbers:

(703) 872-9306 (for formal communication intended for entry);

(703) 746-5429 (for informal or draft communication, please label "PROPOSED" or "DRAFT").

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

TUAN DAM
SUPERVISORY PATENT EXAMINER

TTV

November 26, 2003